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10/775,216	02/11/2004	Teruo Okada	040057	9967

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EXAMINER	
AMRANY, ADI	

ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/775,216	OKADA ET AL.	
	Examiner	Art Unit	
	ADI AMRANY	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/18/08, 8/1/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on July 29, 2008, PROSECUTION IS HEREBY REOPENED. A new rejection of the claims is set forth below in view of the foreign references cited in the Information Disclosure Statements (July 18 and August 1, 2008) under §103(a).

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Michael J Sherry/

Supervisory Patent Examiner, Art Unit 2836

Claim Objections

2. Claim 29 is objected to because the phrase, "individually generating a plurality of DC voltages" is unclear. It appears that applicants are reciting that each power source

circuit can output more than one voltage. Figure 1, however, clearly shows that each circuit provides one voltage

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 29-34, 36 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tominaga (US 5,237,208) in view of Takahashi (US 5,768,117), JP H01-077071 ("JP" microfilm of H03-018681) and Takeaki (JP 01-231622). The last two references were supplied by the applicants in an IDS which contained a listing of references cited by the Japanese Patent Office. The disclosures, relevance or combination of the references were not addressed or rebutted by the applicants in their IDS submission.

With respect to claim 29, Tominaga discloses a multiple output power source apparatus (fig 1) comprising a plurality of power source circuits (items 1, 2, and 3, and col. 5, lines 4-9), each circuit being equipped with an independent output control circuit (fig 2, and col. 5, lines 22-26), wherein each of the output control circuits comprise:

a shutdown circuit (fig 2, items 34, 38; col. 6, lines 9-22 and 48-52) that detects an abnormality of the own power source circuit to output an abnormality signal to control circuits of one or a plurality of other power source circuits via a

first terminal (item 20) and inputting an abnormality signal via the first terminal (20) to shut down the own power source circuit when an abnormality is detected in the own power source circuit;

each of the output control circuits being operably coupled to each other (fig 1, items 6-7, 17 and 20).

Tominaga does not expressly disclose:

A. the power source circuits generate a DC voltage;

B. each power source circuit generates a different DC voltage;

C. the own power source circuit and the other power source circuits simultaneously shut down when an abnormality is detected either in the own power source circuit or in the other power source circuits.

A. Takahashi discloses a multiple output power source apparatus (fig 1; col. 4, 7) comprising a plurality of power source circuits (con1-con4) generating DC voltages (col. 7, lines 6-11). Takahashi also discloses that AC/DC converters may be placed at an input bus (fig 15).

Tominaga and Takahashi are analogous because they are from the same field of endeavor, namely parallel power supplies. At the time of the invention by applicants, it would have been obvious to one skilled in the art to combine the Tominaga power source circuit with the Takahashi rectifier in order to supply power to a DC load. This limitation would be obvious because it is drawn to the end use of the apparatus (powering AC or DC loads).

B. JP discloses that a plurality of parallel power source circuits can each supply power to a different load (fig 2). Tominaga, Takahashi, and JP are analogous because they are from the same field of endeavor, namely parallel power supplies. At the time of the invention by applicants, it would have been obvious to combine the parallel converters disclosed in Tominaga and Takahashi with the multiple outputs disclosed in JP in order to supply power to more than one load. Takahashi also discloses that multiple loads may be connected to the output power bus (fig 9, 15, 19-21).

C. JP (abstract) and Takeaki (abstract) disclose a multiple output power source apparatus wherein all power source circuits simultaneously shut down when an abnormality is detected either in the own power source circuit or the other power source circuit. Takeaki clearly states that in the event of an abnormality in any power source circuit (own circuit or the other circuit), all power source circuits are shutdown.

Tominaga, Takahashi, JP and Takeaki are analogous because they are from the same field of endeavor, namely parallel power supplies. At the time of the invention by applicants, it would have been obvious to combine the parallel converters disclosed in Tominaga and Takahashi with the simultaneous shutdown disclosed in JP and Takeaki in order to prevent errors from damaging the rest of the apparatus.

With respect to claim 30, Tominaga discloses a converter (item 26) that is driven by a switching circuit (item 31), converts an input voltage into a prescribed output voltage.

With respect to claim 31, Tominaga discloses the output stabilizing circuit (col. 5, lines 50-62; col. 6, lines 23-30) comprises:

a reference voltage generating circuit (item 31); an output voltage monitoring circuit (item 32); an oscillator (item 29); and a driving circuit (item 30) that controls the clock signal; and

the shutdown circuit comprises an abnormality detecting circuit (items 34, 38) that is connected to a first terminal of the other power source circuits (col. 5, lines 22-26), outputs an abnormality signal when an abnormality is detected (col. 6, lines 9-13), inputs an abnormality signal (col. 6, lines 14-22), and stops oscillation when an abnormality is detected (col. 7, lines 6-29).

With respect to claim 32, Tominaga discloses an oscillator in the master circuit is connected to an output circuit of a slave circuit via a second terminal, and outputs a synchronous oscillation signal (col. 7, lines 33-42), and an oscillator in an output circuit of the slave is connected to the output circuit of the master via a third terminal, and inputs the synchronous oscillation signal from the master to perform synchronous control (col. 7, lines 43-55). Tominaga does not expressly disclose the process of selecting a master or the slave. Prager discloses one of the plurality of power source circuits is set as a master and one or the plurality of power source circuits except the master is set as a slave (col. 5, lines 48-59).

With respect to claim 33, Tominaga, Takahashi, JP and Takeaki disclose the DC output, the shutdown circuit, the master/slave synchronizing as discussed above in the rejections of claims 29 and 32.

With respect to claim 34, Tominaga discloses a converter and switching circuit (items 26, 31) and the master/slave switching signal synchronization (col. 7, lines 33-55), as discussed above in the rejection of claims 30 and 32, respectively.

With respect to claim 36, Tominaga, Takahashi, JP and Takeaki disclose a converter and switching circuit (claim 30), master/slave synchronizing (claim 32), the master circuit comprises an first oscillator, a stabilizing circuit and a shutdown circuit (claim 31), and the slave circuit comprising a second oscillator, stabilizing circuit, and shutdown circuit (claim 31), as discussed above

With respect to claim 38, Tominaga discloses outputting the abnormality signal when a prescribed voltage is superposed on the synchronous line (col. 8, lines 5-34).

5. Claims 29-32, 35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tominaga in view of Takahashi, JP, Takeaki and Luo (US 1005/0073783).

With respect to claims 29-32, Tominaga, Takahashi, JP and Takeaki disclose the recited limitations, as discussed above. Tominaga discloses that "a terminal" is a port where multiple lines are connected (fig 2, item 20). The terminal connects multiple components, but the terminal itself is one device ("a" terminal). Luo meets the other possible interpretation of "a terminal," in which the connection includes only one line. Luo discloses a multiple output power source apparatus (fig 1; par 32) comprising a plurality of power source circuits (items 10N), wherein the abnormality signal is output and input via a first terminal (connection between circuit 10 and communication line 23).

Tominaga, Takahashi, JP, Takeaki and Luo are analogous because they are from the same field of endeavor, namely parallel power systems. At the time of the invention by applicants, it would have been obvious to one skilled in the art to combine the power source apparatus disclosed in Tominaga, Takahashi, JP and Takeaki with the abnormality communication line disclosed in Luo in order to monitor the status of the other power source circuits.

With respect to claim 35, Tominaga, Takahashi, JP and Takeaki disclose the converter and switching circuit (items 26, 31; claim 30), a stabilizing circuit (item 30; claim 31), a shutdown circuit (item 38; col. 6, lines 1-22), and master/slave output control circuit synchronization (col. 7, lines 33-55; claim 32). The references do not expressly disclose that the master outputs the abnormality signal by stopping the synchronous oscillation signal.

Luo discloses a multiple output power source apparatus (fig 1; par 32) comprising a plurality of power source circuits (items 10N), a stabilizing circuit (fig 1, item 22; figure 3b; pars 35, 38), wherein the master outputs an abnormality signal by stopping the synchronous signal (par 92, lines 5-8).

With respect to claim 37, Tominaga discloses the shutdown circuits measure time during detection of an abnormality signal and cause the power circuit to be shut down when the measured time is a prescribed time or longer (fig 3, item 58; fig 5, item 74; col. 7, lines 23-29; col. 8, lines 29-34). Tominaga does not expressly disclose the master and slave circuits output the abnormality signal when the synchronous line is

grounded. Luo discloses the abnormality signal is transmitted when the synchronous line is grounded, as discussed above in the rejection of claim 35.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ADI AMRANY whose telephone number is (571)272-0415. The examiner can normally be reached on Mon-Thurs, from 10am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J Sherry/
Supervisory Patent Examiner, Art Unit 2836

AA